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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,517	12/09/2003	Erik S. Jeng	386998041US	3730

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EXAMINER	
LEE, EUGENE	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 08/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/731,517	JENG, ERIK S.	
	Examiner	Art Unit	
	Eugene Lee	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 25 July 2006.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-52 is/are pending in the application.

4a) Of the above claim(s) 9-12 and 25-52 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-8,13-24 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 5/23/06 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 5, 13, and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Chang et al. 5,969,383. Chang discloses (see, for example, FIG. 1) an NVM cell (nonvolatile memory device) 10 comprising a semiconductor substrate 11, dielectric layer of silicon dioxide layer (gate oxide) 14, gate (control gate structure) 16, silicon dioxide layer (first isolation layer) 23, silicon nitride layers/silicon dioxide layers (dielectric spacer) 24/28, source/drain (source and drain regions) 36, 22, silicide structures (salicide) 42, 44, 46. The charge trapping capability is the silicon nitride layers 24.

Regarding the limitation "control gate structure", even though Chang calls the gate 16 a select gate, this limitation is descriptive in nature and does not **structurally** differentiate Chang's

invention from the applicant's invention. Chang and the applicant's invention disclose the same structural gate wherein the gate is formed above a substrate surrounded by spacers. The limitation "control" is only a label that does not structurally differentiate Chang's invention. Also, Chang discloses (see, for example, column 1, lines 44-46) that the select gate "controls" the channel current, and, therefore, has a controlling function and may be construed as a "control gate".

Regarding the limitation "wherein said spacer trapping structure includes charge trapping capability thereby storing single or multiple bits of data", it has been held that the recitation that an element is "capable of" performing a function is not a positive limitation but only requires the ability to so perform. It does not constitute a limitation in any patentable sense. In re Hutchison, 69 USPQ 138. In this case, Chang discloses (see, for example, FIG. 1) an NVM cell wherein the NVM cell contains two ONO stacks 28. Each of these ONO stacks are capable of storing a bit. Further, on column 3, lines 21-23, Chang discloses that charge carriers are injected into the ONO stack 25 and trapped in charge trapping sites formed in the silicon nitride layer 24. This is exactly the same function used for the nitride spacers 12 as shown in FIG. 1 of applicant's figures, and described (i.e. nitride spacers are used to trap carriers … used to store charges) in paragraph [0039] of the applicant's specification.

Regarding claim 5, see, for example, FIG. 1 wherein Chang discloses a silicon nitride layer (second isolation layer) 24.

Regarding claim 14, see, for example, FIG. 1 wherein Chang discloses an NVM cell (nonvolatile memory device) 10 comprising a semiconductor substrate 11, dielectric layer of silicon dioxide layer (gate oxide) 14, gate (gate structure) 16, silicon dioxide layer (first isolation

layer) 23, nitride spacers (dielectric spacer) 34, 35, source/drain (source and drain regions) 36, 22, silicide structures (salicide) 42, 44, 46.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2, 3, 6, 7, and 15 thru 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. '383 as applied to claims 1, 5, 9, 13, and 14 above, and further in view of Zheng et al. 6,762,085 B2. Chang does not disclose a pocket implantation region. However, Zheng discloses (see, for example, FIG. 10) a first region 30 comprising an N type source/drain region 9, and a p type halo region (pocket implantation region) 7. In column 3, lines 44-53, Zheng discloses the halo region reducing the risk of punch through, or leakage. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have a pocket implantation region in order to reduce the risk of punch through, or leakage.

Regarding claim 3, Chang does not disclose a lightly doped drain region. However, Zheng discloses (see, for example, FIG. 10) a first region 30 comprising an N type LDD region (lightly doped drain region) 8. It would have been obvious to one of ordinary skill in the art at time of invention to have a lightly doped drain region in order to relax the electric field and reduce leakage current.

Regarding claims 6, and 7, see, for example, FIG. 1 wherein Chang discloses a silicon nitride layer (second isolation layer) 24.

Regarding claims 15, 18, and 21, Chang does not disclose the silicide material including $TiSi_2$, $CoSi_2$, or NiSi. However, Zheng discloses (see, for example, FIG. 10, and column 5, lines 27-29) silicide layers 16 comprising titanium silicide, cobalt silicide, and nickel silicide. It would have been obvious to one of ordinary skill in the art at the time of invention to have the silicide material including $TiSi_2$, $CoSi_2$, or NiSi since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice (In re Leshin, 125 USPQ 416) in order to have an adequate conductive material that reduces parasitic resistance.

Regarding claims 17, and 20, see, for example, FIG. 1 wherein Chang discloses an NVM cell (nonvolatile memory device) 10 comprising a semiconductor substrate 11, dielectric layer of silicon dioxide layer (gate oxide) 14, gate (gate structure) 16, silicon dioxide layer (first isolation layer) 23, nitride spacers (dielectric spacer) 34, 35, source/drain (source and drain regions) 36, 22, silicide structures (salicide) 42, 44, 46.

6. Claims 4, 8, and 22 thru 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. '383 as applied to claims 1, 5, 13, and 14 above, and further in view of Kasuya 6,784,078 B2, and further in view of Zheng et al. 6,762,085 B2. Chang does not disclose a double doped drain region. However, Kasuya discloses (see, for example, Fig. 1) a semiconductor device comprising a high concentration impurity diffusion region 44, and a low concentration impurity diffusion region (double doped drain region) 42. It would have been

obvious to one of ordinary skill in the art at the time of invention to have a double doped drain region in order to enclose the source/drain region, and reduce leakage current.

Chang in view of Kasuya does not disclose a pocket implantation region. However, Zheng discloses (see, for example, FIG. 10) a first region 30 comprising an N type source/drain region 9, and a p type halo region (pocket implantation region) 7. In column 3, lines 44-53, Zheng discloses the halo region reducing the risk of punch through, or leakage. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have a pocket implantation region in order to reduce the risk of punch through, or leakage.

Regarding claim 8, see, for example, FIG. 1 wherein Chang discloses silicon nitride layer (second isolation layer) 24.

Regarding claim 23, see, for example, FIG. 1 wherein Chang discloses an NVM cell (nonvolatile memory device) 10 comprising a semiconductor substrate 11, dielectric layer of silicon dioxide layer (gate oxide) 14, gate (gate structure) 16, silicon dioxide layer (first isolation layer) 23, nitride spacers (dielectric spacer) 34, 35, source/drain (source and drain regions) 36, 22, and silicide structures (salicide) 42, 44, 46.

Regarding claim 24, Chang in view of Kasuya does not disclose the silicide material including $TiSi_2$, $CoSi_2$, or NiSi. However, Zheng discloses (see, for example, FIG. 10, and column 5, lines 27-29) silicide layers 16 comprising titanium silicide, cobalt silicide, and nickel silicide. It would have been obvious to one of ordinary skill in the art at the time of invention to have the silicide material including $TiSi_2$, $CoSi_2$, or NiSi since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the

intended use as a matter of obvious design choice (In re Leshin, 125 USPQ 416) in order to have an adequate conductive material that reduces parasitic resistance.

Response to Arguments

7. Applicant's arguments filed 7/25/06 have been fully considered but they are not persuasive.

Regarding applicant's argument on page 15, last paragraph that the split-gate FET structure of Chang is structurally different from the nonvolatile memory of the present invention, this argument is not persuasive. Even though there are structural differences between the FET structure of Chang and the applicant's invention, these structural differences are not made distinct in the applicant's claims. In column 1, lines 44-46, Chang discloses that the select gate "controls" the channel current, and, therefore, has a controlling function and may be construed as a "control gate". Further, Chang discloses (see, for example, column 3, lines 21-23) that charge carriers are injected into the ONO stack 25 and trapped in charge trapping sites formed in the silicon nitride layer 24. This is exactly the same function used for the nitride spacers 12 (as shown in FIG. 1 of applicant's figures), and described (i.e. nitride spacers are used to trap carriers … used to store charges) on paragraph [0039] of the applicant's specification. Therefore, these nitride spacers have charge trapping capability in the same manner as stated in the applicant's claims.

INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 571-272-1733. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Eugene Lee
August 25, 2006

EUGENE LEE
PRIMARY EXAMINER